Analysis of Switching Table Based Three Level Diode Clamped Multilevel Inverter

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Abstract: **This paper proposes a switching table based three level diode clamped multilevel inverter (DCMLI). The proposed control method determines the sector and the voltage vector are selected from switching table. It is used to generate gating signals for the inverter. The 2-level inverter and 3-level DCMLI are analysed. This can be extended to n-level inverter. The total harmonic distortion (THD) and fundamental voltages are computed and compared. The results show that the performance is improved. The significant feature of the proposed method is its simplicity. Simulations were performed for these two inverters using MATLAB/SIMULINK and the results are presented. The relative advantages are highlighted.**

***Index Terms*—Two Level Inverter, Three Level Inverter, Multi Level Inverter, DCMLI.**

I. INTRODUCTION

Most of the industrial applications drives are the Induction motor drives with voltage source inverters. The voltage waveforms of two level inverter fed Induction motor shows that the voltage across the motor contains not only the fundamental component, also harmonics voltage. The rate of change of voltage dv/dt is very high.The voltage stress on the power semiconductor devices is very high. So it is not advisable to retain the 2-levelconfiguration for higher voltage motors. The high and medium voltage induction motors are generally controlled using three level inverters. The 3-Level inverter, on the other hand, allows the motor voltage to go up in steps. This reduces the dv/dt stress for the same DC bus voltage V_{dc}. Inverters of higher number of levels such as 5and 7 level can also be constructed. However, the circuit assembly becomes very complex and issues such as keeping all the sections of the dc bus voltage equal have to be addressed [1]. The general structure of the multilevel converter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. As the number of levels increases, the output waveform adds more steps, producing a staircase waveform which approaches the sinusoidal wave with less harmonic distortion. The stepped waveform is obtainedby selecting different voltage levels generated by the proper connection of the load to the different capacitive voltage sources. This connection is performed by the proper switching of the power semiconductors.

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There are three main topologies of multilevel inverters. The diode clamped multilevel inverter (DCMLI), flying capacitor multilevel inverter (FCMLI) and cascaded H-bridge multilevel inverter (CHBMLI). Comparing the devices and components used, the diode clamped inverter requires more number of diodes and the flying capacitor inverter requires more number of capacitors while the cascaded H-bridge inverter requires less number [4].

The commonly used modulation techniques are multilevel sinusoidal pulse width modulation (SPWM) [11], multilevel selective harmonic elimination pulse width modulation (SHEPWM) [13] and space vector pulse width modulation (SVPWM) [15]. In multilevel SPWM, a sinusoidal reference waveform is compared with triangular carrier waveforms to generate switching sequence. It requires more number of carrier waveforms in different levels [16]. In SHEPWM, the transcendental equations characterizing harmonics are solved to compute switching angles, which are difficult to solve [17]. In SVPWM the complexity is due to the difficulty of determining the location of the reference vector, the calculation of on-times, the determination and selection of switching states and the existence of many redundant switching vectors as the number of levels increases [18]. A simple control method for multilevel inverter is the switching table based control method. In this paper the diode clamped multilevel inverter is considered to explain this control method since it is the common multilevel inverters used in many applications. This paper presents a switching table based 2-level inverter and 3-level diode clamped multilevel inverter. Section II presents the sector identification, switching table and the output phase voltages and line voltages of two level inverter and section 3 presents the three level diode clamped inverters. The Simulation results are presented in section IV. The performance comparison of two level inverter and three level diode clamped inverter are included.

II. TWO LEVEL INVERTER

The three phase 2-level inverters are used in many applications. A three phase output can be obtained from a configuration of six devices as shown in figure 1 [25]. Three devices are remains on at any instant. The on state is represented by 1 and off state is represented 0. The devices S_{a1}', S_{b1}' and S_{c1}' are complementary to S_{a1}, S_{b1} and S_{c1}respectively. S_{a1}'=1–S_{a1}, S_{b1}'=1–S_{b1} and S_{c1}'=1–S_{c1}. There are eight combinations which produce eight voltage vectors. The voltage vectors are from V_0, V_1, V_2, V_3, V_4, V_5, V_6, $V_7$and V_8. V_1 to V_6 are nonzero vectors and V_0 and V_7 is the zero vectors.

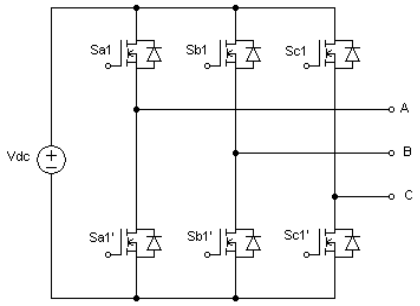


Figure 1: 2-Level Inverter

One cycle is divided into six sectors with 60° each. The angle and the corresponding sector and the voltage vector are given in table I. The vector sequence is $V_1 \rightarrow V_2 \rightarrow V_3 \rightarrow V_4 \rightarrow V_5 \rightarrow V_6 \rightarrow V_1$.

TABLEI
SECTORSAND VOLTAGE VECTORS

Sector	Angle	Voltage Vector
1	$0^o \leq \theta \leq +60^o$	V_1
2	$+60^o \leq \theta \leq +120^o$	V_2
3	$+120^o \leq \theta \leq +180^o$	V_3
4	$-180^o \leq \theta \leq -120^o$	V_4
5	$-120^o \leq \theta \leq -60^o$	V_5
6	$-60^o \leq \theta \leq 0^o$	V_6

The three phase voltages can be represented in two phase. The coordinate transformation is obtained using the following equations (1) and (2).

$$\boldsymbol{v_q = \frac{2}{3}\left[v_a - \frac{1}{2}(v_b + v_c)\right]} \quad (1)$$

$$\boldsymbol{v_d = \frac{1}{\sqrt{3}}(v_b - v_c)} \quad (2)$$

Using equations (1) and (2), and the line voltage as reference, the d-q components of the rms voltage the d-q line voltages can be expressed as in equations (3) and (4).

$$\boldsymbol{v_{lq} = \sqrt{\frac{3}{2}}\frac{2}{3}\left[v_a - \frac{1}{2}(v_b + v_c)\right]} \quad (3)$$

$$\boldsymbol{v_{ld} = \sqrt{\frac{3}{2}}\frac{1}{\sqrt{3}}(v_b - v_c)} \quad (4)$$

The angle can be found using equation (5).

$$\boldsymbol{\theta = \tan^{-1}\left(\frac{v_{ld}}{v_{lq}}\right)} \quad (5)$$

The switching table is formed using θ. If, $0^o \leq \theta \leq +60^o$ it is in sector 1. It selects the voltage vector V_1. The corresponding switching state is 100. The switching table is given in table II.

TABLE II
SWITCHING TABLE

Sec.	Vect.	Switch State					
		S_{a1}	S_{b1}	S_{c1}	S_{a1}'	S_{b1}'	S_{c1}'
1	V_1	1	0	0	0	1	1
2	V_2	0	1	0	1	0	1
3	V_3	0	0	1	1	1	0
4	V_4	1	0	1	0	1	0
5	V_5	1	1	0	0	0	1
6	V_6	0	1	1	1	0	0
Note: $S_{a1}'=1-S_{a1}$, $S_{b1}'=1-S_{b1}$ and $S_{c1}'=1-S_{c1}$							

In sector 1, the phase voltages are given by,

$$\boldsymbol{v_{an} = +\frac{V_s}{3}, v_{bn} = -\frac{2V_s}{3} \text{ and } v_{cn} = +\frac{V_s}{3}}$$

The phase voltages for all sectors are given in table III.

TABLE III
PHASE VOLTAGES

Sector	Phase Voltage		
	v_{an}	v_{bn}	v_{cn}
1	$+\frac{V_s}{3}$	$-\frac{2V_s}{3}$	$+\frac{V_s}{3}$
2	$+\frac{2V_s}{3}$	$-\frac{V_s}{3}$	$-\frac{V_s}{3}$
3	$+\frac{V_s}{3}$	$+\frac{V_s}{3}$	$-\frac{2V_s}{3}$
4	$-\frac{V_s}{3}$	$+\frac{2V_s}{3}$	$-\frac{V_s}{3}$
5	$-\frac{2V_s}{3}$	$+\frac{V_s}{3}$	$+\frac{V_s}{3}$
6	$-\frac{V_s}{3}$	$-\frac{V_s}{3}$	$+\frac{2V_s}{3}$

In sector 1, the line voltages are given by,

$$v_{ab} = +V_s, v_{bc} = 0 \text{ and } v_{ca} = -V_s$$

The line voltages for all sectors are given in table IV.

TABLE IV
LINE VOLTAGES

Sector	Line Voltages		
	v_{ab}	v_{bc}	v_{ca}
1	$+V_s$	0	$-V_s$
2	0	$+V_s$	$-V_s$
3	$-V_s$	$+V_s$	0
4	$-V_s$	0	$+V_s$
5	0	$-V_s$	$+V_s$
6	$+V_s$	$-V_s$	0

The line voltage has two levels. The simulation of two level inverter is given the section 5.

III. THREE LEVEL DIODE CLAMPED INVERTER

The three phase 3-level diode clamped multilevel inverter is the common multilevel inverter used for various applications [18]. A three phase three level diode clamped inverter is obtained from a configuration of twelve switching devices as shown in figure 2. The devices S_{a1}', S_{a2}', S_{b1}', S_{b2}', S_{c1}' and S_{c2}' are complementary to S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{c1} and S_{c2}. $S_{a1}'=1-S_{a1}$, $S_{a2}'=1-S_{a2}$, $S_{b1}'=1-S_{b1}$, $S_{b2}'=1-S_{b2}$, $S_{c1}'=1-S_{c1}$ and $S_{c2}'=1-S_{c2}$. The twelve active combinations were taken.

The voltage vectors are from V_1, V_2, V_3, V_4, V_5, V_6, V_7, V_8, V_9, V_{10}, V_{11}, and V_{12}.

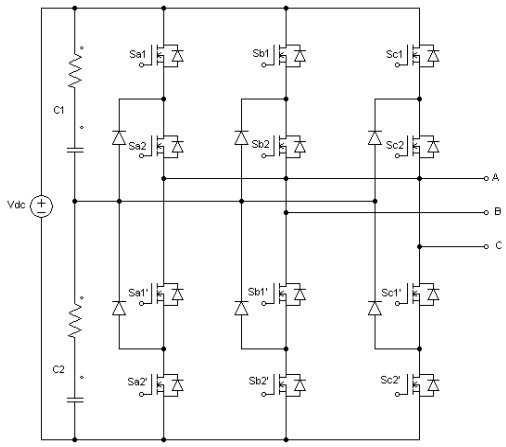


Figure 2: Three Level Diode Clamped Inverter

One cycle is divided into twelve sectors with 30° each. The angle and the corresponding sector and the voltage vector are given in table V. The vector sequence is $V_1 \rightarrow V_2 \rightarrow V_3 \rightarrow V_4 \rightarrow V_5 \rightarrow V_6 \rightarrow V_7 \rightarrow V_8 \rightarrow V_9 \rightarrow V_{10} \rightarrow V_{11} \rightarrow V_{12} \rightarrow V_1$.

TABLEV
SECTORSAND VOLTAGE VECTORS

Sector	**Angle**	**Voltage Vector**
1	$0^o \leq \theta \leq +30^o$	V_1
2	$+30^o \leq \theta \leq +60^o$	V_2
3	$+60^o \leq \theta \leq +90^o$	V_3
4	$+90^o \leq \theta \leq +120^o$	V_4
5	$+120^o \leq \theta \leq +150^o$	V_5
6	$+150^o \leq \theta \leq +180^o$	V_6
7	$-180^o \leq \theta \leq -150^o$	V_1
8	$-150^o \leq \theta \leq -120^o$	V_2
9	$-120^o \leq \theta \leq -90^o$	V_3
10	$-90^o \leq \theta \leq -60^o$	V_4
11	$-60^o \leq \theta \leq -30^o$	V_5
12	$-30^o \leq \theta \leq 0^o$	V_6

The switching table is formed using θ. If, $0^o \leq \theta \leq +30^o$it is in sector 1. It selects the voltage vector V_1. The corresponding switching state is 110000.The switching table is given in table VI.

TABLEVI
SWITCHING TABLE

Sec.	Vect.	Switch State					
		S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}
1	V_1	1	1	0	0	0	0
2	V_2	1	1	0	1	0	0
3	V_3	1	1	1	1	0	0
4	V_4	0	1	1	1	0	0
5	V_5	0	0	1	1	0	0
6	V_6	0	0	1	1	0	1
7	V_7	0	0	1	1	1	1
8	V_8	0	0	0	1	1	1
9	V_9	0	0	0	0	1	1
10	V_{10}	0	1	0	0	1	1
11	V_{11}	1	1	0	0	1	1
12	V_{12}	1	1	0	0	0	1
Note: S_{a1}'=1–S_{a1}, S_{a2}'=1–S_{a2}, S_{b1}'=1–S_{b1}, S_{b2}'=1–S_{b2},S_{c1}'=1–S_{c1} and S_{c2}'=1–S_{c2}							

In sector 1, the phase voltages are given by,

$$\boldsymbol{v_{an} = +\frac{2V_s}{3}, v_{bn} = -\frac{V_s}{3} \text{ and } v_{cn} = -\frac{V_s}{3}}$$

The phase voltages for all sectors are given in table VII.

TABLEVII
PHASE VOLTAGES

Sector	Phase Voltage		
	v_{an}	v_{bn}	v_{cn}
1	$+\frac{2V_s}{3}$	$-\frac{V_s}{3}$	$-\frac{V_s}{3}$
2	$+\frac{V_s}{2}$	0	$-\frac{V_s}{2}$
3	$+\frac{V_s}{3}$	$+\frac{V_s}{3}$	$-\frac{2V_s}{3}$
4	0	$+\frac{V_s}{2}$	$-\frac{V_s}{2}$
5	$-\frac{V_s}{3}$	$+\frac{2V_s}{3}$	$-\frac{V_s}{3}$
6	$-\frac{V_s}{2}$	$+\frac{V_s}{2}$	0
7	$-\frac{2V_s}{3}$	$+\frac{V_s}{3}$	$+\frac{V_s}{3}$
8	$-\frac{V_s}{2}$	0	$+\frac{V_s}{2}$
9	$-\frac{V_s}{3}$	$-\frac{V_s}{3}$	$+\frac{2V_s}{3}$
10	0	$-\frac{V_s}{2}$	$+\frac{V_s}{2}$
11	$+\frac{V_s}{3}$	$-\frac{2V_s}{3}$	$+\frac{V_s}{3}$
12	$+\frac{V_s}{2}$	$-\frac{V_s}{2}$	0

In sector 1, the line voltages are given by,

$$\boldsymbol{v_{ab} = +V_s, v_{bc} = 0 \text{ and } v_{ca} = -V_s}$$

The line voltages for all sectors are given in table VIII.

TABLEVIII
LINE VOLTAGES

Sector	Line Voltages		
	v_{ab}	v_{bc}	v_{ca}
1	$+V_s$	0	$-V_s$
2	$+\frac{V_s}{2}$	$+\frac{V_s}{2}$	$-V_s$
3	0	$+V_s$	$-V_s$
4	$-\frac{V_s}{2}$	$+V_s$	$-\frac{V_s}{2}$
5	$-V_s$	$+V_s$	0
6	$-V_s$	$+\frac{V_s}{2}$	$+\frac{V_s}{2}$

7	$-V_s$	0	$+V_s$
8	$-\frac{V_s}{2}$	$-\frac{V_s}{2}$	$+V_s$
9	0	$-V_s$	$+V_s$
10	$+\frac{V_s}{2}$	$-V_s$	$+\frac{V_s}{2}$
11	$+V_s$	$-V_s$	0
12	$+V_s$	$-\frac{V_s}{2}$	$-\frac{V_s}{2}$

The line-to-line voltage has three levels. The simulation of three level diode clamped inverter is given the next section.

IV. SIMULATION RESULTS

The simulations of two level inverter and three level diode clamped inverter are carried out with dc supply of 400 V. The phase and line voltage waveforms are plotted. The fundamental output voltages and total harmonic distortion are found and tabulated.

The sectors are identified as discussed in section II and III. The sector identification is shown in figure 3 and 4. The phase voltage waveforms are shown in figure 5(a) and (b). The FFT analyses of phase voltage waveform are given in figure 6(a) and (b). The line voltage waveforms are shown in figure 7(a) and (b). The FFT analyses of phase voltage waveform are given in figure 8(a) and (b).

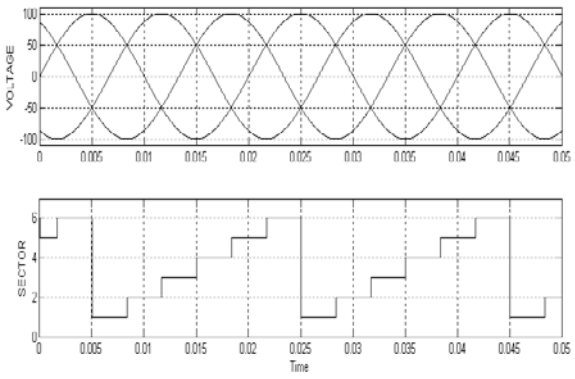


Figure 3: Sector Identification – Two Level Inverter

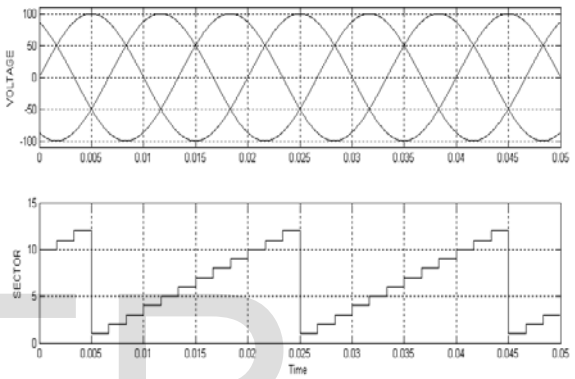
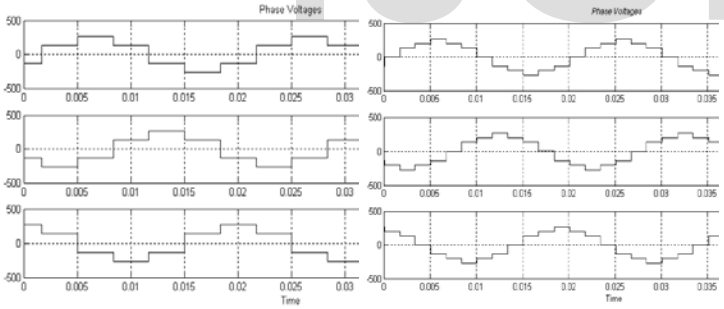
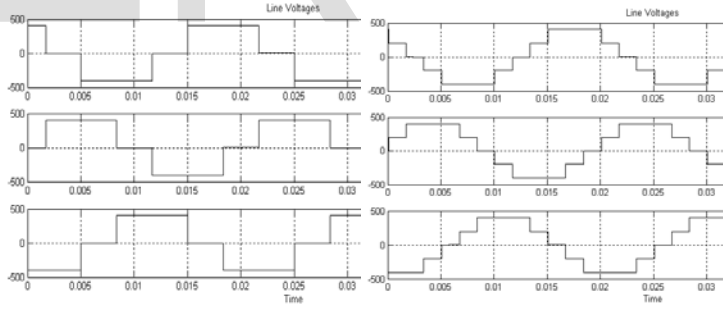


Figure 4: 3-Level Inverter Sector Identification



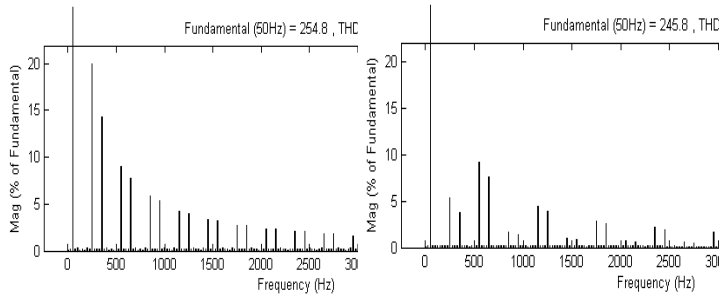
(a) (b)

Figure 5: Phase Voltages (a) Two Level Inverter (b) Three Level Diode Clamped Inverter



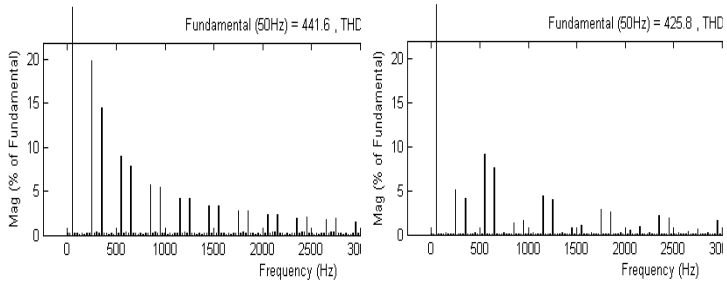
(a) (b)

Figure 7: Line Voltages (a) Two Level Inverter (b) Three Level Diode Clamped Inverter



(a) (b)

Figure 6: FFT Analysis of Phase Voltages (a) Two Level Inverter (b) Three Level Diode Clamped Inverter



(a) (b)

Figure 8: FFT Analysis of Line Voltages (a) Two Level Inverter (b) Three Level Diode Clamped Inverter

Figure 6(a) and (b) shows the FFT analysis of the phase voltage of two level and three level diode clamped inverter respectively. The fundamental phase voltage of two level inverter is 254.8V and three level inverter 245.8V. The total harmonic distortion is 30.79% and 16.79%. Figure 8(a) and (b) shows the FFT analysis of the line voltages of two level and three level diode clamped inverter respectively.The fundamental line voltage of two level inverter 441.6V and three level inverter is 425.8V. The total harmonic distortion is 30.75% and 16.78%. The FFT analysis of two level inverter and three level diode clamped inverter are summarized in table IX.

TABLEIX
LINE VOLTAGES

Inverter	Phase Voltage	Line Voltage
	Fundamental Voltage	
2-level	254.8V	441.6V
3-level	245.8V	425.8V
	Total Harmonic Distortion	
2-level	30.79%	30.75%
3-level	16.79%	16.78 %

The simulation results show that harmonics are very much reduced and the fundamental voltages are slightly reduced in three level diode clamped inverter.

V. CONCLUSION

This paper provides the analysis of switching table based two level inverter and three level diode clamped inverter. A particular emphasis on total harmonic distortion and fundamental voltages has been studied. The simulation results show that increasing the number levels of inverter can achieve low total harmonic distortion. The presented switching table based three level diode clamped can be easily implemented.

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